WHAT IS CLAIMED IS:

1. An inkjet printhead comprising:

an internal power supply path;

a power regulator providing an offset voltage from the internal power supply path voltage; and

multiple primitives, each primitive including:

a group of nozzles;

a corresponding group of firing resisters; and

a corresponding group of switches controllable to couple a selected firing resister of the group of firing resisters between the internal power supply path and the offset voltage to thereby permit electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

2. The inkjet printhead of claim 1 wherein the power regulator is a linear power regulator.

3. The inkjet printhead of claim 1 wherein each switch includes a field effect transistor (FET).

4. The inkjet printhead of claim 1 wherein the power regulator includes:

a digital-to-analog converter (DAC) coupled to the internal power supply path and configured to receive a digital offset command representing a desired offset voltage and to provide an analog offset voltage from the internal power supply path voltage.

5. The inkjet printhead of claim 4 wherein the power regulator further includes:

a buffer amplifier configured to receive the analog offset voltage and to provide a buffered offset voltage.

6. The inkjet printhead of claim 5 wherein the power regulator further includes:

multiple feedback amplifiers corresponding to the multiple primitives, each feedback amplifier receiving the buffered offset voltage and providing the offset voltage to a corresponding primitive.

7. The inkjet printhead of claim 6 wherein the printhead further comprises:

an internal power ground;

wherein each feedback amplifier includes a first input coupled to the buffered offset voltage, a second input coupled to the offset voltage, and an output; and

wherein the power regulator further includes:

multiple transistors, each transistor coupled between the internal power ground and the offset voltage and having a gate coupled to the output of a corresponding feedback amplifier.

8. The inkjet printhead of claim 7 wherein each transistor is a field effect transistor (FET).

9. The inkjet printhead of claim 6 wherein the printhead further comprises:

an internal power ground; and

wherein each feedback amplifier includes a first input coupled to the buffered offset voltage, a second input coupled to a feedback line, and an output coupled to a drive line;

wherein each firing resister in a primitive includes a first terminal coupled to the internal power supply path and a second terminal;

wherein the group of switches in each primitive include subgroups of switches, each subgroup of switches corresponding to a firing resister and including:

a power transistor coupled between the second terminal of the firing resister and the internal power ground and having a control gate;

a first switch coupled between the drive line and the control gate of the power transistor; and

a second switch coupled between the feedback line and the second terminal of the firing resistor.

10. The inkjet printhead of claim 9 wherein the power transistor is a field effect transistor (FET).

11. The inkjet printhead of claim 4 wherein the DAC is a current-mode DAC.

12. The inkjet printhead of claim 4 further comprising:
a processor supplying the digital offset command.

13. An inkjet printhead assembly comprising:
at least one printhead, each printhead including:
an internal power supply path;
a power regulator providing an offset voltage from the internal power supply path voltage; and
multiple primitives, each primitive including:
a group of nozzles;
a corresponding group of firing resisters; and
a corresponding group of switches controllable to couple a selected firing resister of the group of firing resisters between the internal power supply path and the offset voltage to thereby permit electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

14. The inkjet printhead assembly of claim 13 wherein the at least one printhead includes multiple printheads.

15. An inkjet printing system comprising:

a first power supply;

at least one printhead, each printhead including:

an internal power supply path coupled to the first power supply;

a power regulator providing an offset voltage from the internal power supply path voltage; and

multiple primitives, each primitive including:

a group of nozzles;

a corresponding group of firing resisters; and

a corresponding group of switches controllable to couple a selected firing resister of the group of firing resisters between the internal power supply path and the offset voltage to thereby permit electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

16. The inkjet printing system of claim 15 wherein the power regulator includes:

a digital-to-analog converter (DAC) coupled to the internal power supply path and configured to receive a digital offset command representing a desired offset voltage and to provide an analog offset voltage from the internal power supply path voltage.

17. The inkjet printing system of claim 16 wherein the power regulator further includes:

a buffer amplifier configured to receive the analog offset voltage and to provide a buffered offset voltage.

18. The inkjet printing system of claim 17 wherein the power regulator further includes:

multiple feedback amplifiers corresponding to the multiple primitives, each feedback amplifier receiving the buffered offset voltage and providing the offset voltage to a corresponding primitive.

19. The inkjet printing system of claim 18 wherein the printing system further comprises:

a first power ground; and

wherein the printhead further includes:

an internal power ground coupled to the first power ground;

wherein each feedback amplifier includes a first input coupled to the buffered offset voltage, a second input coupled to the offset voltage, and an output; and

wherein the power regulator further includes:

multiple transistors, each transistor coupled between the internal power ground and the offset voltage and having a gate coupled to the output of a corresponding feedback amplifier.

20. The inkjet printing system of claim 18 wherein the printing system further comprises a first power ground, and wherein the printhead further includes:

an internal power ground coupled to the first power ground;

wherein each feedback amplifier includes a first input coupled to the buffered offset voltage, a second input coupled to a feedback line, and an output coupled to a drive line;

wherein each firing resister in a primitive includes a first terminal coupled to the internal power supply path and a second terminal;

wherein the group of switches in each primitive include subgroups of switches, each subgroup of switches corresponding to a firing resister and including:

a power transistor coupled between the second terminal of the firing resister and the internal power ground and having a control gate;

a first switch coupled between the drive line and the control gate of the power transistor; and

a second switch coupled between the feedback line and the second terminal of the firing resistor.

21. The inkjet printing system of claim 16 wherein the printhead further includes:

a processor supplying the digital offset command.

22. The inkjet printing system of claim 16 further comprising:

an electronic controller supplying the digital offset command to the printhead.

23. A method of inkjet printing in an inkjet printhead comprising:

providing an internal power supply path;

providing an offset voltage from the internal power supply path voltage;

coupling a selected firing resister of a group of firing resisters between the internal power supply path and the offset voltage to cause electrical current to pass through the selected firing resister to cause a corresponding selected nozzle to fire.

24. The method of claim 23 wherein providing the offset voltage includes:

converting a digital offset command representing a desired offset voltage to an analog offset voltage from the internal power supply path voltage.

25. The method of claim 24 wherein providing the offset voltage further includes:

buffering the analog offset voltage.

26. The method of claim 25 wherein providing the offset voltage further includes:

receiving the buffered analog offset voltage at a feedback amplifier; and

providing the offset voltage with the feedback amplifier.

27. The method of claim 24 further comprising:

supplying the digital offset command.